WHAT IS CLAIMED IS:

1. A multilevel metal interconnect formed on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer;

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers; and

a capacitive structure formed between adjacent metal lines of a patterned metal layer, the capacitive structure being formed from a dielectric material, the dielectric material being different from one of the layers of insulation material.

2. The multilevel metal interconnect of claim 1 and further comprising a plurality of trenches formed in the layers of insulation material each trench adjoining metal lines of the top patterned metal layer, a trench extending from the top metal layer between metal lines of the top metal layer through the top insulation layer and between

metal lines of a metal layer lying below the top metal layer, each trench having a bottom surface.

3. The multilevel metal interconnect of claim 2 wherein the bottom surface has a single level.

4. The multilevel metal interconnect of claim 2 wherein the bottom surface has multiple levels.

5. The multilevel metal interconnect of claim 1 wherein the bottom surface of the trench is spaced apart from a top surface of the semiconductor substrate.

6. The multilevel metal interconnect of claim 1 wherein the dielectric material includes a plurality of layers of dielectric material.

7. The multilevel metal interconnect of claim 1 wherein the capacitive structure has a layer of material formed to adjoin a layer of insulation material, the layer of material being different from the layer of insulation material.

8. The multilevel metal interconnect of claim 1 wherein the capacitive structure is formed adjacent to a trench.

9. The multilevel metal interconnect of claim 1 wherein the capacitive structure is formed between a pair of adjacent trenches.

10. The multilevel metal interconnect of claim 1 wherein a first trench is filled with air and a second trench is filled with the capacitive structure.

11. A method of forming a multilevel metal interconnect on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

a plurality of layers of insulation material, the plurality of layers of insulation material including a first layer of insulation material and a top layer of insulation material, the first layer of insulation material being formed on the semiconductor substrate;

a corresponding plurality of patterned metal layers formed on the layers of insulation material so that each patterned metal layer is formed on a corresponding layer of insulation material, the plurality of patterned metal layers including a first patterned metal layer and a top patterned metal layer, the first patterned metal layer being formed on the first layer of insulation material;

a plurality of contacts formed through the first layer of insulation material to make electrical connections with the active areas and the first patterned metal layer; and

a plurality of vias formed through the plurality of layers of insulation material other than the first layer of insulation material, the vias making electrical connections with adjacent patterned metal layers,

the method comprising the steps of:

etching the layers of insulation material exposed between metal lines in the top patterned metal layer for a predetermined period of time to form a plurality of trenches, each trench being substantially straight; and

forming a layer of dielectric material in the trenches.

12. The method of claim 10 wherein each trench has a bottom surface.

13. The method of claim 11 wherein the bottom surface has a single level.

14. The method of claim 11 wherein the bottom surface has multiple levels.

15. The method of claim 11 wherein the bottom surface of the trench is spaced apart from a top surface of the semiconductor substrate.

16. The method of claim 10 wherein the step of forming a layer of dielectric material includes the steps of:

forming a layer of first dielectric material in the trenches; and

forming a layer of second dielectric material on the layer of first dielectric material.

17. The method of claim 10 and further comprising the steps of:

forming a mask on the layer of dielectric material to protect a capacitor region of the layer of dielectric material and define exposed regions of the layer of dielectric material; and

etching the exposed regions of the layer of dielectric material for a predetermined period of time to form a capacitive structure in a trench.

18. The method of claim 16 and further comprising the step of etching the layer of dielectric material for a predefined time prior to forming the mask.

19. The method of claim 16 wherein the capacitive structure is formed adjacent to a trench.

20. The method of claim 16 wherein the capacitive structure is formed between a pair of adjacent trenches.

21. The method of claim 16 wherein a first trench is filled with air and the capacitive structure is formed in a second trench.

22. The multilevel metal interconnect of claim 1 wherein the trenches are substantially straight.

23. The multilevel metal interconnect of claim 1 wherein a first trench contacts a second trench.

24. The method of claim 11 wherein the etching the layers of insulation material step is substantially anisotropic.

25. A method of forming a multilevel metal interconnect on a semiconductor substrate, the semiconductor substrate having a plurality of active areas, the multilevel metal interconnect comprising:

forming a layer of insulation material over a patterned metal layer;

etching a capacitor region on the layer of insulation material to form a trench;

forming a dielectric material in the trench, the dielectric material being different from the layer of insulation material; and

forming vias in the layer of insulation material.